

WHAT IS CLAIMED IS:

- 1 1. A method of fabricating a semiconductor device, the method comprising:
2 providing a workpiece;
3 disposing a first dielectric material over the workpiece;
4 disposing a second dielectric material over the first dielectric material, the second
5 dielectric material comprising a different material than the first dielectric material, wherein the
6 first dielectric material and the second dielectric material comprise a first insulating layer; and
7 forming a first pattern in the first dielectric material and a second pattern in the second
8 dielectric material, the second pattern being different from the first pattern.
- 1 2. The method according to Claim 1, wherein the second dielectric material comprises a top
2 surface, further comprising:
3 depositing a conductive material over the patterned second dielectric material and the
4 patterned first dielectric material; and
5 removing the conductive material from the top surface of the second dielectric material.
- 1 3. The method according to Claim 2, wherein removing the conductive material from the
2 top surface of the second dielectric material comprises forming conductive lines in the second
3 pattern of the second dielectric material.
- 1 4. The method according to Claim 2, wherein the conductive material forms vias in the first
2 pattern of the first dielectric material.
- 1 5. The method according to Claim 4, wherein the vias comprise substantially vertical
2 sidewalls.

- 1 6. The method according to Claim 4, wherein the workpiece comprises component regions,
2 wherein at least one of the vias makes electrical contact with a component region of the
3 workpiece.
- 1 7. The method according to Claim 6, wherein the workpiece component regions comprise a
2 plurality of conductive lines formed in a dielectric layer.
- 1 8. The method according to Claim 7, wherein the conductive lines comprise copper,
2 wherein disposing the first dielectric material comprises disposing a material having a coefficient
3 of thermal expansion (CTE) close to the CTE of the first conductive lines.
- 1 9. The method according to Claim 1, further comprising:
2 depositing a hard mask over the second dielectric material.
- 1 10. The method according to Claim 9, wherein depositing the hard mask comprises:
2 depositing a first mask layer;
3 depositing a second mask layer over the first mask layer; and
4 depositing a third mask layer over the second mask layer.
- 1 11. The method according to Claim 10, wherein depositing the first mask layer comprises
2 depositing SiC_x , SiC_xN_y , SiC_xH_y , $\text{SiC}_x\text{N}_y\text{H}_z$, or SiCOH , wherein depositing the second mask
3 layer comprises depositing Si_xN_y or SiO_2 , and wherein depositing the third mask layer comprises
4 depositing a refractory metal nitride.
- 1 12. The method according to Claim 11, wherein depositing the first mask layer comprises
2 depositing a layer of SiC_x and a layer of N-SiC_x over the layer of SiC_x .

1 13. The method according to Claim 10, wherein forming the first pattern and the second
2 pattern comprises:
3 patterning at least the third mask layer with the second pattern;
4 patterning the third mask layer, the second mask layer and the first mask layer with the
5 first pattern;
6 transferring the first pattern to the second dielectric material;
7 removing the third mask layer, the second mask layer and the first mask layer in the
8 second pattern regions;
9 transferring the first pattern to the first dielectric material; and
10 removing the second dielectric material in the second pattern regions.

1 14. The method according to Claim 13, further comprising disposing the semiconductor
2 device in a processing chamber before disposing the first dielectric material over the workpiece;
3 and before removing the second dielectric in the second pattern regions, cleaning the processing
4 chamber while the wafer remains in the processing chamber without etching a material layer of
5 the semiconductor wafer.

1 15. The method according to Claim 14, wherein cleaning the processing chamber comprises
2 introducing a plasma cleaning gas comprising O₂ gas diluted in Ar, He, or N₂, and wherein the
3 plasma cleaning gas removes polymer build-up on the processing chamber walls.

1 16. The method according to Claim 15, further comprising only applying power to an
2 electrode in the chamber during cleaning, wherein the workpiece is not biased during the
3 cleaning method, and wherein the plasma electrode power density applied comprises about 0.1
4 W/cm² to 10 W/cm² at a pressure of about 50 mTorr to 500 mTorr.

1 17. The method according to Claim 13, further comprising, before removing the second
2 dielectric in the second pattern regions, moving the workpiece to a clean processing chamber.

1 18. The method according to Claim 13, further comprising:
2 depositing a cap layer over the workpiece, before disposing the first dielectric material;
3 and
4 transferring the first pattern to the cap layer.

1 19. The method according to Claim 18, further comprising forming an adhesion film over a
2 top surface of the cap layer.

1 20. The method according to Claim 1, further comprising forming an adhesion film disposed
2 over a top surface of the first dielectric layer.

1 21. The method according to Claim 13, wherein forming the first pattern and the second
2 pattern further comprises:
3 after patterning at least the third mask layer with the second pattern, depositing an anti-
4 reflective coating over the third mask layer;
5 depositing a photoresist layer over the anti-reflective coating;
6 patterning the photoresist layer with the first pattern; and
7 transferring the first pattern in the photoresist layer to the third mask layer, the second
8 mask layer, the first mask layer, and the second dielectric layer.

1 22. The method according to Claim 1, wherein disposing the first dielectric material
2 comprises disposing an inorganic material, and wherein disposing the second dielectric material
3 comprises disposing an organic material.

1 23. The method according to Claim 1, wherein disposing the first dielectric material
2 comprises disposing a material that is etchable selective to the second dielectric material.

1 24. The method according to Claim 1, wherein disposing the first dielectric material
2 comprises disposing undoped silicate glass (USG), fluorinated silicon glass (FSG), fluorinated
3 tetraethoxysilate (FTEOS), SiCOH, or porous-SiCOH, and wherein disposing the second
4 dielectric material comprises disposing SiLKTM or porous-SiLKTM.

1 25. A method of fabricating a semiconductor device, the method comprising:
 2 providing a workpiece;
 3 forming a first insulating layer over the workpiece;
 4 forming a plurality of first conductive lines in the first insulating layer;
 5 disposing a first dielectric material over the first insulating layer;
 6 disposing a second dielectric material over the first dielectric material, the second
 7 dielectric material comprising a different material than the first dielectric material, wherein the
 8 first dielectric material and the second dielectric material comprise a second insulating layer;
 9 forming a first pattern in the first dielectric material and a second pattern in the second
 10 dielectric material, the second pattern being different from the first pattern;
 11 depositing a conductive material over the patterned second dielectric material and the
 12 patterned first dielectric material; and
 13 removing the conductive material from the top surface of the second dielectric material to
 14 form a plurality of second conductive lines in the second pattern of the second dielectric material
 15 and a plurality of vias in the first pattern of the first dielectric material.

1 26. The method according to Claim 25, wherein forming the vias comprises forming vias
 2 with substantially vertical sidewalls.

1 27. The method according to Claim 25, wherein at least one of the vias makes electrical
 2 contact to a first conductive line.

1 28. The method according to Claim 25, wherein disposing the first dielectric material
 2 comprises disposing an inorganic material, and wherein disposing the second dielectric material
 3 comprises disposing an organic material.

- 1 29. The method according to Claim 25, wherein disposing the first dielectric material
2 comprises disposing a material that is etchable selective to the second dielectric material.
- 1 30. The method according to Claim 25, wherein disposing the first dielectric material
2 comprises disposing undoped silicate glass (USG), fluorinated silicon glass (FSG), fluorinated
3 tetraethoxysilate (FTEOS), SiCOH, or porous-SiCOH, and wherein disposing the second
4 dielectric material comprises disposing SiLKTM or porous-SiLKTM.
- 1 31. The method according to Claim 25, wherein the first conductive lines comprise copper,
2 wherein disposing the first dielectric material comprises disposing a material having a coefficient
3 of thermal expansion (CTE) close to the CTE of the first conductive lines.
- 1 32. The method according to Claim 25, further comprising:
2 depositing a hard mask over the second dielectric material.
- 1 33. The method according to Claim 32, wherein depositing the hard mask comprises:
2 depositing a first mask layer;
3 depositing a second mask layer over the first mask layer; and
4 depositing a third mask layer over the second mask layer.
- 1 34. The method according to Claim 33, wherein depositing the first mask layer comprises
2 depositing SiC_x, SiC_xN_y, SiC_xH_y, SiC_xN_yH_z, or SiCOH, wherein depositing the second mask
3 layer comprises depositing Si_xN_y or SiO₂, and wherein depositing the third mask layer comprises
4 depositing a refractory metal nitride.
- 1 35. The method according to Claim 34, wherein depositing the first mask layer comprises
2 depositing a layer of SiC_x and a layer of N-SiC_x over the layer of SiC_x.

1 36. The method according to Claim 33, wherein forming the first pattern and the second
2 pattern comprises:
3 patterning at least the third mask layer with the second pattern;
4 patterning the third mask layer, the second mask layer and the first mask layer with the
5 first pattern;
6 transferring the first pattern to the second dielectric material;
7 removing the third mask layer, the second mask layer and the first mask layer in the
8 second pattern regions;
9 transferring the first pattern to the first dielectric material; and
10 removing the second dielectric material in the second pattern regions.

1 37. The method according to Claim 36, further comprising disposing the semiconductor
2 device in a processing chamber before disposing the first dielectric material over the workpiece;
3 and before removing the second dielectric in the second pattern regions, cleaning the processing
4 chamber while the wafer remains in the processing chamber without etching a material layer of
5 the semiconductor wafer.

1 38. The method according to Claim 37, wherein cleaning the processing chamber comprises
2 introducing a plasma cleaning gas comprising O₂ gas diluted in Ar, He or N₂, and wherein the
3 plasma cleaning gas removes polymer build-up on the processing chamber walls.

1 39. The method according to Claim 38, further comprising only applying power to an
2 electrode in the chamber during cleaning, wherein the workpiece is not biased during the
3 cleaning method, and wherein the plasma electrode power density applied comprises about 0.1
4 W/cm² to 10 W/cm² at a pressure of about 50 mTorr to 500 mTorr.

1 40. The method according to Claim 36, further comprising, before removing the second
2 dielectric in the second pattern regions, moving the workpiece to a clean processing chamber.

1 41. The method according to Claim 36, wherein forming the first pattern and the second
2 pattern further comprises:

3 after patterning at least the third mask layer with the second pattern, depositing an anti-
4 reflective coating over the third mask layer;

5 depositing a photoresist layer over the anti-reflective coating;

6 patterning the photoresist layer with the first pattern; and

7 transferring the first pattern in the photoresist layer to the third mask layer, the second
8 mask layer, the first mask layer, and the second dielectric layer.

1 42. The method according to Claim 25, further comprising:

2 depositing a cap layer over the workpiece, before disposing the first dielectric material;

3 and

4 transferring the first pattern to the cap layer.

1 43. The method according to Claim 42, further comprising forming a first adhesion film over
2 a top surface of the cap layer and forming a second adhesion film over a top surface of the first
3 dielectric material.

1 44. A method of cleaning a chamber that has been used to etch inorganic materials in
2 semiconductor device fabrication, the chamber having polymer build-up on the interior walls
3 thereof, the method comprising:

4 without removing a semiconductor wafer that has been processed in the chamber,
5 introducing a plasma cleaning gas into the chamber to remove the polymer build-up on the
6 chamber walls without etching a material layer of the semiconductor wafer.

1 45. The method according to Claim 44, wherein introducing the plasma cleaning gas
2 comprises introducing a gas comprising O₂ gas diluted in Ar, He or N₂.

1 46. The method according to Claim 45, wherein introducing the plasma cleaning gas
2 comprises introducing a gas comprising an O₂ concentration of about 1% to 20%.

1 47. The method according to Claim 44, further comprising only applying power to an
2 electrode in the chamber during cleaning, and wherein the wafer is not biased during the cleaning
3 method.

1 48. The method according to Claim 47, wherein the plasma electrode power density applied
2 comprises about 0.1 W/cm² to 10 W/cm² at a pressure of about 50 mTorr to 500 mTorr.

1 49. The method according to Claim 44, wherein the semiconductor wafer comprises a hard
2 mask formed thereon, wherein the hard mask is not etched or removed during the cleaning
3 method.